Application Note

Application Note

AN1121

G32A14xx Series Application Note

Version: V1.1

1 Introduction

This application note provides precautions to be taken when using the G32A14xx series.

Contents

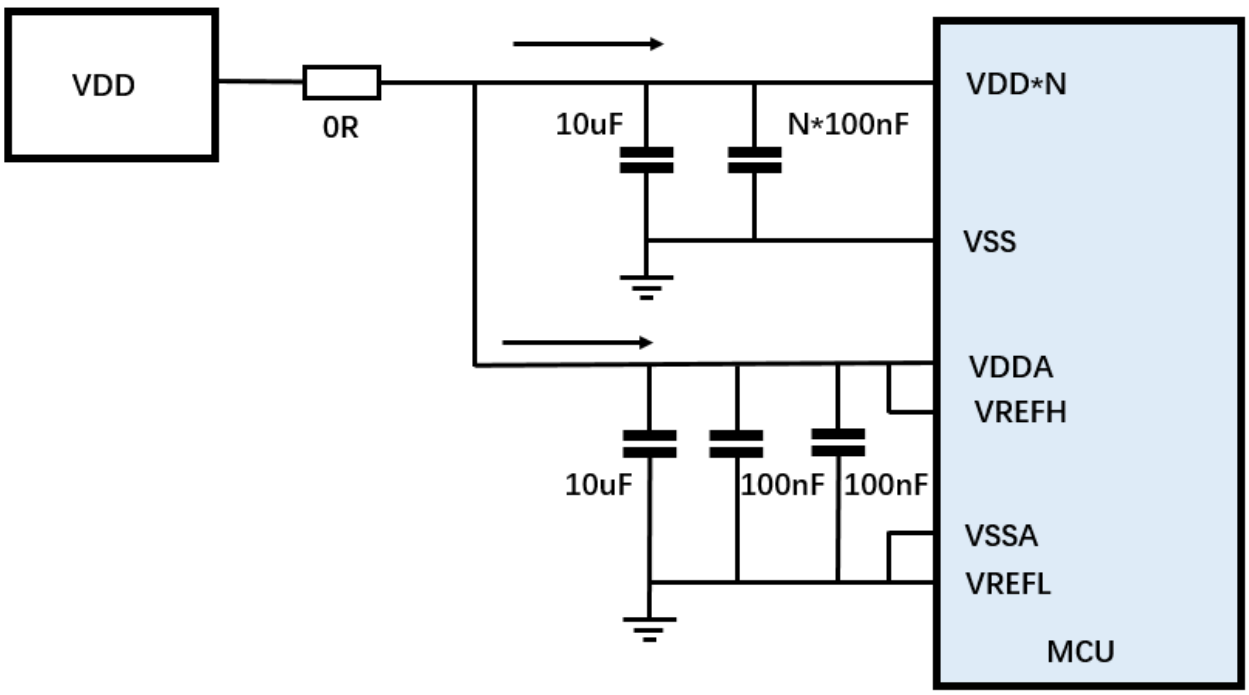
2 Note to Hardware Application Design

2.1 Design of MCU Filter Capacitor

The chip power ports (VDD, VSS) need to be connected in parallel to large and small filter capacitors, as shown in Figure 1, where N is the number of VDD PIN for each package. The effectiveness of capacitors depends on the optimal placement and connection type. PCB layout requires star-shaped wiring, and it is important to note that the external power supply passes through large and small capacitors and then connects to the chip. The large and small filter capacitors should be placed as close to the chip as possible within 4mm.

The resistor 0R shown in Figure 1 can be replaced with magnetic beads, and the EMI test item (RE) can add the test margin, which can refer to the parameters 600R@100MHz.

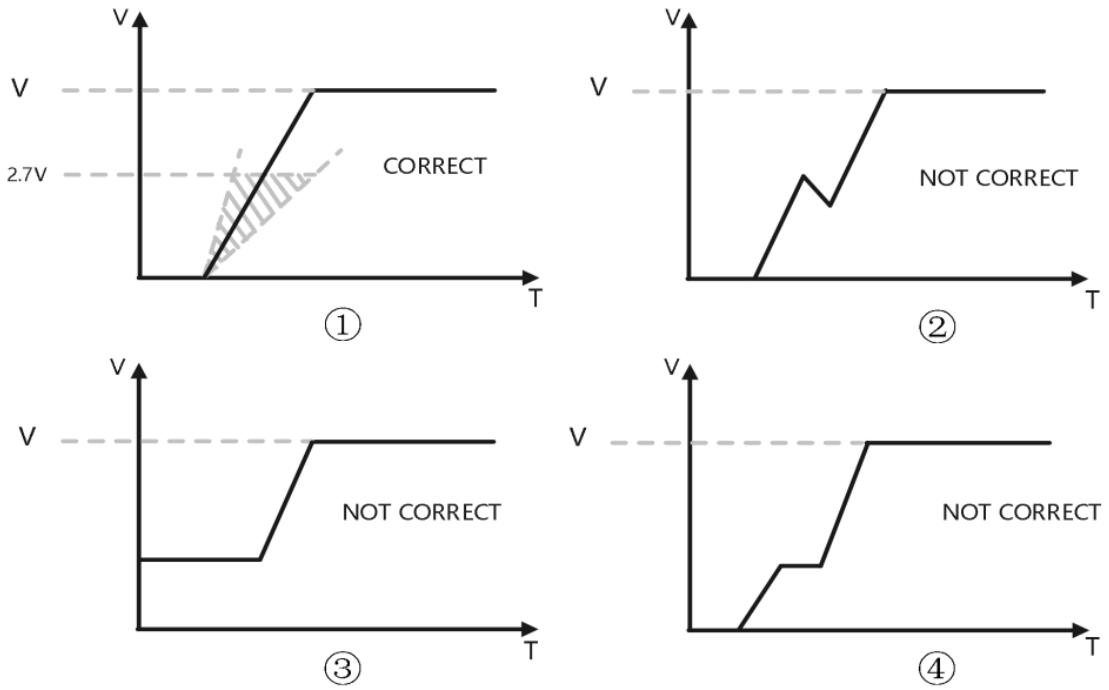
Figure 1 Design of Filter Capacitors



2.2 Precautions for MCU Power Supply

The MCU's power supply ramp rate should meet the maximum and minimum value limits specified in the datasheet, namely greater than 0.5V/min and less than 100V/ms respectively. It takes at least 55us to increase from 0V to 5.5V, and at least 27us to increase from 0V to 2.7V. Too high or too low power-on rate may cause the MCU to fail to work normally; MCU needs to be powered down to below 300mV before being powered on again, and the above time must meet the requirements within the full temperature range. The power-on startup waveform needs to meet the waveform ① in Figure 2, while the other three waveforms are incorrect.

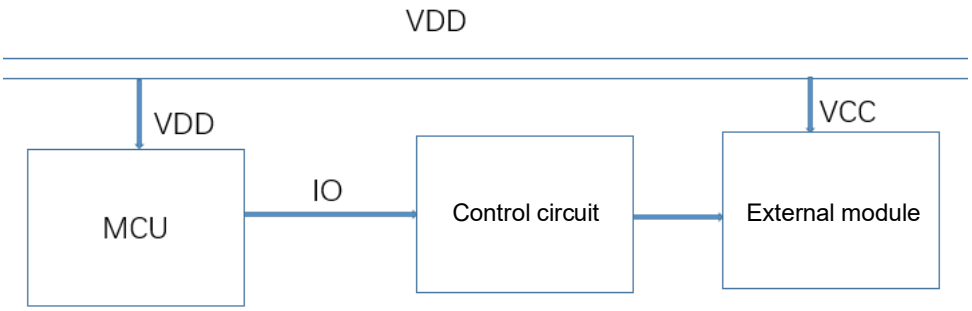
Figure 2 Power-on Waveform



2.3 The peripheral module uses VDD and VSS

When MCU is used to control the power supply or power-on process of external modules, too high power-on rate should be avoided to prevent the problem of VDD voltage being pulled down due to sudden current changes. To ensure stable operation of the system and protect the circuit from potential damage, it is recommended to adopt appropriate delay measures for steady power supply conversion. The power-on speed can be adjusted by adding appropriate buffer elements, such as capacitors or resistors, so that voltage dip will not be caused to VDD due to instantaneous high current demand. If sudden dip is caused for this reason, the drop speed must also meet the requirements of the ECU's power supply ramp rate. (Use examples shown in Figures 3 and 4)

Figure 3 IO Control Peripheral Module

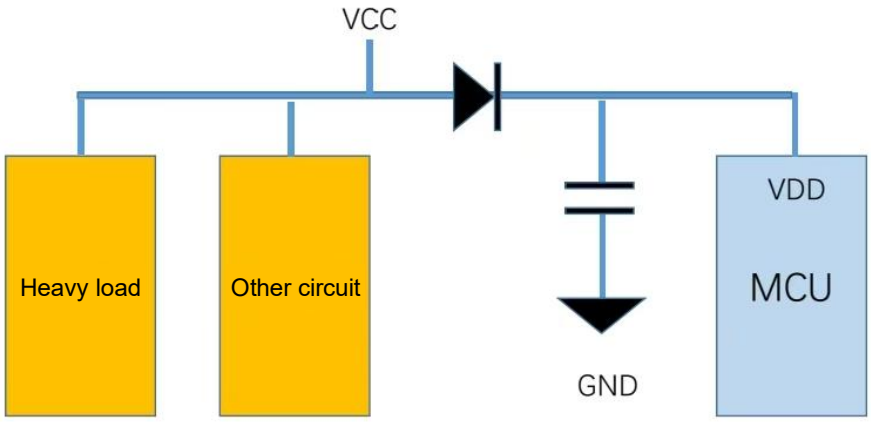


In order to avoid power fluctuation, in applications where MCU power supply is above 3.6V, connect a low voltage-drop diode in series on the circuit or connect a 10R resistor in series and a capacitor of above 10uF in parallel to form a fast power drop protection circuit. If the capacitance

is large enough, the power down will be slow and the power-down magnitude can be very small.

Note: If the germanium diode conducts, there will be a voltage drop of 0.2V, which will reduce the power supply of the MCU by 0.2V compared to before. If ADC/DAC is used, the accuracy may be affected.

Figure 4 Shared Power Supply for Peripherals



2.4 External and High-frequency Signals

- Attention should be paid to checking whether an instantaneous increase in load may be caused by zero-crossing signals, relay signals, AC loads, etc. The load impact can be mitigated by bypass capacitors.
- Attention should be paid to whether instantaneous peak currents will be generated in high-frequency IIC clock lines, high-frequency SPI clock lines, CAN high-frequency signal lines (CANH and CANL lines), etc.

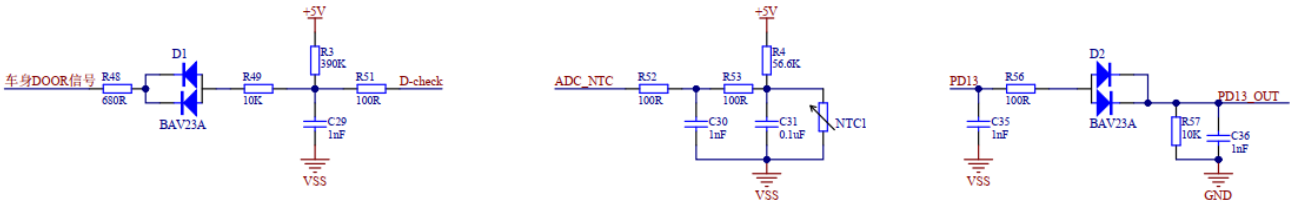
2.5 Connect the Input/Output signal port to a current limiting resistor in series and connect the capacitor to VSS in parallel

For Input/Output ports (e.g. ADC, external interrupts, communication interfaces, etc.), it is recommended to connect to the protective resistors in series in circuit design. The resistance value should be considered and calculated, and the theoretical maximum current should not exceed the limit parameters that the chip port can withstand; the resistors connected in series and capacitors connected in parallel should be placed as close as possible to the chip pins, and the resistors should be connected in series before the capacitors are connected in parallel. The ground of the filter capacitor of the peripheral module must be connected to the ground that has passed through the large and small filter capacitors (VDD, VSS). Figure 5 shows an example of resistor and capacitor connection of the body DOOR signal, ADC detection, and IO_OUT. The IO port is connected to a 100R resistor in series and a 1nF capacitor in parallel.

Note that in the design of PCB interconnection (similar to separating lamps from control modules, separating sensors from control modules), this series-connected resistors and parallel-connected capacitors should be placed on the PCB board of the chip. Reasonable parameters and placement positions can effectively prevent damage to

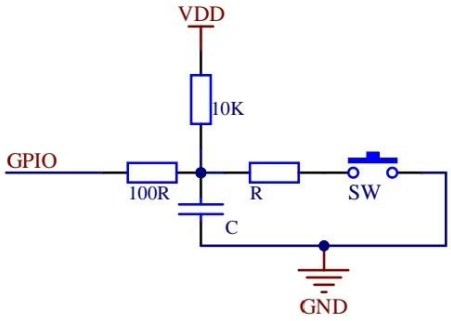
the chip ports by ESD/EOS.

Figure 5 Circuit Example of Body DOOR Signal/ADC Detection/IO_OUT



For button circuits, the recommendations are as follows:

Figure 6 Button Circuit



It is recommended to use a 220nF capacitor for C in Figure 6, and a small resistor R, e.g. 1k or 100R, can be connected in series next to the button. At the same time, the capacitor C should be placed close to the button SW when designing the PCB. So that it can avoid the negative impact pressure generated by buttons.

2.6 IO voltage cannot be higher than VDD voltage

When the IC is not powered by VDD, but there is voltage at the IO port, this voltage will be supplied to the IC through a pull-up protection diode. Or when the IC is powered by VDD, but there is a higher voltage at the IO port than VDD, the voltage difference between this voltage and VDD will cause the pull-up protection diode to conduct, making the current flow into VDD. Under normal circumstances, IO cannot exceed 0.3V above VDD.

This phenomenon can easily cause the following hazards:

(1) Too high current will cause the clamp diode on the IO port to quickly overload and be damaged.

(2) It will make MCU reset unsuccessfully.

(3) It will cause disorder in the chip program.

(4) A latch-up effect will result.

2.7 Precautions for IO Sink Current

When IO is used to drive external circuits, attention should be paid to the current limit parameters in the specifications, including without limitation:

(1) IOL, IO sink current, typical sink current that can be output by IO port.

(2) IOH, IO source current, typical source current that can be output by IO port.

(3) IOLS, IO strong sink current, typical strong sink current that can be output by IO port.

(4) IOHS, IO strong source current, typical strong source current that can be output by IO port.

Exceeding the range specified by the limit parameters will cause damage to the chip, and it is impossible to predict the working state of the chip outside the above indicated range. Moreover, if the chip operates under conditions outside the indicated range for a long time, the reliability of the chip may be affected.

2.8 Pay Attention to Protection for Exposed Ports

- For communication ports, ESD protection measures are required. A small resistor 100R can be connected in series on the signal line to limit the amplitude of ESD current; transient voltage suppressor diodes (TVS) can be connected in parallel on the signal line, near the interface position.
- There is a hot-plugging risk in the burning port, and it should be protected by first contacting GND and then contacting IO during the connection.

3 Precautions for Software Application

3.1 Precautions for GPIO Operation

1. Unused GPIO ports should be set to output low level or connect an external 100Ω resistor for pull-down.

2. Different GPIO pins should avoid being configured with the same multiplexing function!

3. When the chip VDD is powered on within the range of 0V-2.7V, the GPIO port is in an uncertain state, and attention should be paid to the impact of unstable condition of GPIO on the stability of the post-stage drive circuit; when VDD is powered on above 2.7V, after the chip completes the power-on reset, the status of the GPIO port will be executed according to the program settings.

3.2 Precautions for using LPO as a clock source (WDT/EWDT/RTC…)

LPO clock accuracy is poor, so it is recommended not to use LPO as a clock source as much as possible. If only LPO can be selected as the clock source, it is recommended to consider the possible accuracy deviation in extreme environments. When LPO clock source is used for WDT, it is recommended to feed the dog at a frequency that is more than twice the set reset time. Assuming the watchdog is set to reset for 2 seconds, it is recommended to feed the dog every 1 second.

3.3 Clock Precautions for PLL

The PLL clock source of G32A14xx can only be an external clock OSC.

PLL cannot be lower than 23MHz.

3.4 Clock Precautions for LSI

LSI is an internal 8MHz clock with a significant error (refer to the description in relevant datasheet for details). In extreme environments, there may be a frequency error of ±10%, so it is recommended to avoid using it in situations where there are requirements for accuracy. Communication peripherals do not use this clock source, and it is recommended to use OSC or PLL clock sources.

3.5 Precautions for I2C

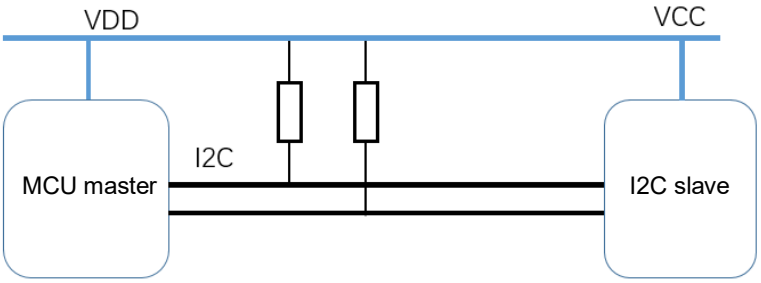
In the process of sudden power failure and recovery of pull-up power supply of SCL/SDA, there is a possibility that the combination of SCL/SDA voltage and logic timing may trigger START but not STOP, resulting in the bus remaining in BUSY state. Recommended avoidance scheme:

1. The pull-up power supply of I2C must be stable to prevent the power supply from dropping too low due to instability during use. For common scenarios of I2C master-slave communication, the following hardware design is recommended:

a. The host and slave share the power supply, as shown in the circuit of Figure 7, where VDD

and VCC are the shared power supply;

Figure 7 I2C Communication Circuit



b. When the host and slave cannot share power supply, it is recommended to connect the power supply of pull-up resistor to the power supply of host MCU, as shown in Figure 7, and connect the pull-up resistor to VDD.

2. The bus can also be released by resetting the slave. If EEPROM is used as a slave, it is impossible to reset the salve using the software, and the bus release function needs to be added to the I2C host when establishing a new communication. Due to the probability of bus locking, the bus BUSY status timeout function can be added. Combination of the two can improve the robustness of the system.

3. If the I2C device on the bus can recognize power failure, turn off the I2C module before power failure.

3.6 Precautions for Erasing FLASH

1. If consecutive multi-page erase operations are required, please ensure that the watchdog count is correctly cleared during the erase period to prevent triggering watchdog reset due to long erasing time.

2. During the FLASH erase and write period, please ensure stable power supply. If the power supply is unstable (e.g. in case of power failure), abnormal operation of the FLASH module will result and errors will appear, and even ECC errors be may be triggered when accessing the FLASH address next time it is powered on. (Voltage monitoring function can be added to the program. If the supply voltage is too low, the operation of FLASH will be stopped.)

3. There is a power-on delay of 100ms before operating on the FLASH and EEPROM.

4. Enable the ECC error interrupt, and erase the wrongly accessed FLASH address in the interrupt to restore access to this FLASH address. Enable ECC interrupt of FLASH to set FLASH_ECFG.DBFIEN to 1, and define the interrupt entry function void FLASH_Fault_IRQHandler().

5. After an ECC error occurs, the data needs to be erased. In order to prevent data loss, the second FLASH sector can be used for data backup. When an ECC error occurs, it can be read from the backup area. After one sector is erased, erase the second FLASH sector. The second

sector will only be read when it is powered on and ECC errors occur. It is important to distinguish ECC errors occur in which flash sector, and the corresponding FLASH sector can be erased. The distinguishing method can be to make a signal mark before reading this address.

3.7 Precautions for Use of Safe Mode

The safe mode of the chip is set by configuring the 0x400-0x40F address area, which is a dedicated 16-byte configuration area used to store some configuration information of security, protection, and MCU startup. The chip configuration is in safe mode, and mass erase is also disabled. At this time, burning tools such as JLINK cannot be used to connect the chip, so it is not possible to decrypt the MCU by entering the command unlock Kinetis to execute the mass erase instruction in the J-LINK commander tool, only the FLASH instruction can be executed, to use the internal instruction Erase All Blocks instruction 0x44 in the chip to erase the program. This instruction can only be executed in the program, and the chip can only be restored in this way to burn the program again.

A program function can be added to the code to execute the Erase All Blocks command instruction 0x44 through hidden serial port instructions or other communication interface instructions in the program to erase the program, which can not only protect the chip from malicious reading of the program, but also restore the chip and lift the safe state in case of program updates. Here are the key codes: (There are relevant codes in the SDK)

```
//Key functions

 STATUS_T FLASH_EraseAllBlock(const FLASH_SSD_CONFIG_T * ssdCfg)

 {

      STATUS_T returnValue;

      /* Check OCIFLG to verify the previous command is completed */

      if(0U != (FLASH->STS.reg & 0x80U)>>7U)

      {

    /* Clear COLEFLG & ACCEFLG & PROVFLG flag in flash status register. Write 1 to clear */

           FLASH->STS.reg = (uint8_t)0x70U;

           FLASH->CCMDDATA0.reg = FTFx_ERASE_ALL_BLOCK;//erase instruction

           /* Execute the command */

           returnValue = FLASH_CommandSequence(ssdCfg);

      }

      else   {
```

```
            returnValue = STATUS_BUSY;
        }
        return returnValue;
    }
    //Related functions
    FUNCTION_DEFINITION_AT_RAMSECTION_START
    static STATUS_T FLASH_CommandSequence(const FLASH_SSD_CONFIG_T * ssdCfg)
    {
        STATUS_T returnValue = STATUS_SUCCESS;
        /* Clear OCIFLG to launch command */
        FLASH->STS.reg = (uint8_t)(0x80U);
        while (((FLASH->STS.reg >> 7U) & 0x01U) == 0)
        {
            /* Wait till OCIFLG bit is set
             * Serve callback function as often as possible
             */
            if(ssdCfg->callBack != CALLBACK_IS_NULL)
            {
                /* Temporarily disable compiler's check for ROM access call from within a ram
function.
                 * The use of a function pointer type makes this check irrelevant.
                 * Nevertheless, it is imperative that the user-provided callback be defined in
RAMSECTION */
                FUNCTION_CALL_AT_RAMSECTION_CHECK_DISABLE
                (ssdCfg->callBack)();
                FUNCTION_CALL_AT_RAMSECTION_CHECK_ENABLE
            }
        }
```

```
        /* Check for protection violation error */
        if ((FLASH->STS.reg & (0x01U | 0x10U |0x20U | 0x40U)) != 0U)
        {
            returnValue = STATUS_ERROR;
        }
        return returnValue;
    }
    FUNCTION_DEFINITION_AT_RAMSECTION_END
```

4 Precautions for Use of Simulators/Burning Tools

4.1 The development environment supports IAR, KEIL, and Eclipse

1. IAR is recommended to use V8.50.5 version and above.

2. KEIL is recommended to use MDK-ARM V5.36 version.

Note: For the projects that fail to compile with a low-version MDK cannot be used after it has been updated to a higher version, the original error project cannot be used, and the SDK program needs to be decompressed again for use.

3. J-Link software is recommended to use 7.96o version and above.

4. Eclipse is recommended to use V2022-06(4.24.0) version and above, and the installation package can be downloaded in Eclipse.

If there is a prompt as follows when compiling with Eclipse:

Cannot run program "make": Launching failed

Error: Program "make" not found in PATH

Solution: Right-click the project and select properties--->C/C++Build--->Tool Chain Editor--->Current builder:

Change the original Gnu Make Builder to CDT Internal Builder, and click OK.

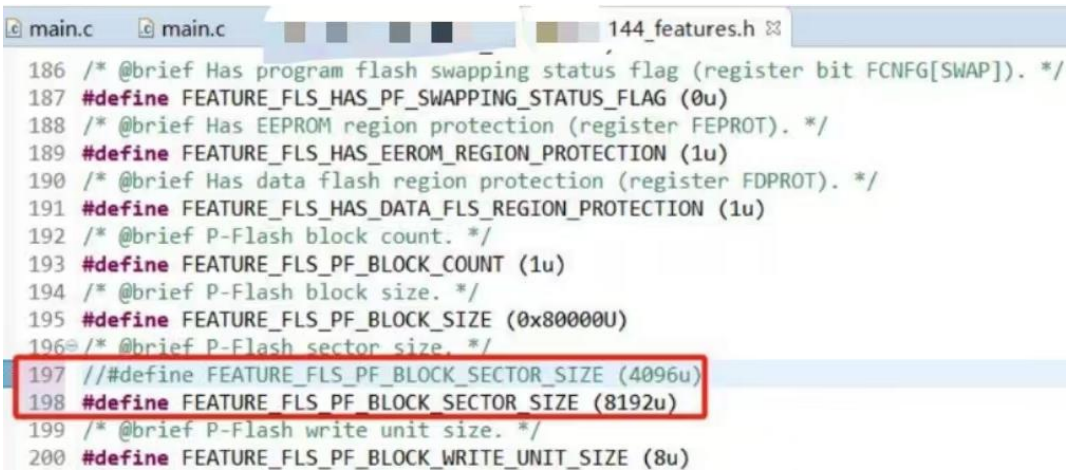
4.2 Other Precautions for Development Environment

When third-party software is used for development (SxxDS), note that one sector of G32A14xx is 8K, while third-party software may operate on 4K or other when erasing.

1. Simulation may be abnormal or impossible. If there is a problem, it can be restored by first burning the program with J-Link/Jflash, and then using PE/J-Link in third-party software for simulation debugging.

2. The sector size of G32A14xx P-flash is 8K. When executing the boot loader upgrade APP segment program, it is necessary to modify the definition of P-flash sector size in order to ensure normal implementation of erasing the original storage area. Modify the xx144_features.h document at the location defined by the red box as shown in Figure 8, and change 4096u to 8192u. After modification, click Save first and then compile; otherwise the latest changes will not be included during compilation.

Figure 8 Modification Location of Features Document



3. When updating the mode for the BootA+BootB+APP code, both the BootB and APP programs need to ensure that the definition rules of start address comply with multiples of 8192 (8K). The start address for storing APP must be a multiple of 8192 (8K), and the start address for storing other information must also be a multiple of 8192 (8K).

5 Revision history

Table 1 Document Revision History

Date	Version	Revision History
December,2024	1.0	New
April,2025	1.1	Added software precautions

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